



**PEDASOFT**

# EM Supreme<sup>®</sup>

Fully Integrated  
EM Simulator for  
RF Components and Modules

[support@pedasoft.com](mailto:support@pedasoft.com)

+1(650)352-3585

ASK for our RF design and Modeling Services!



Introduction

EM-Supreme<sup>®</sup> Overview

Design Flow

PA Example

RF Power Transistor Application

Summary



## ➤ Introduction

EM-Supreme<sup>®</sup> Overview

Design Flow

PA Example

RF Power Transistor Application

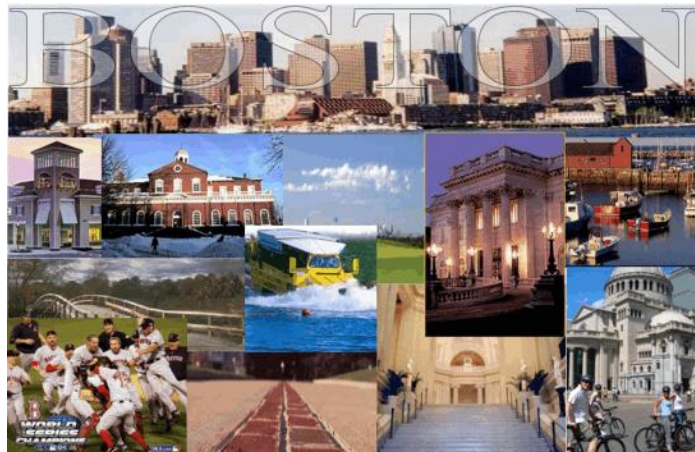
Summary



# INTRODUCTION

## PedaSoft

- Pedasoft LLC was founded in 2006 to create a higher accuracy EM simulation tool in order to reduce the time required to develop RF circuits.
- The EM-Core<sup>®</sup> time domain field solver and the EM-Supreme<sup>®</sup> simultaneous active and passive simulator were unveiled at the 2009 IMS.





# INTRODUCTION

## TRENDS

RF DESIGN CHALLENGES

- Multiband
  - › Number of different radios / wireless devices is **growing**.
- Design Cycles
  - › Time allowed for design is **shrinking**.
- Size
  - › Amount of area for any given function is **shrinking**.
- Clock Speed
  - › IC operating speed is **increasing**.
- Application / Standards Frequency
  - › New applications are **increasing** operating frequency.

MARKET

- Product Lifecycles
  - › Lifetime of any given product is **shrinking**.
- Internet of Things
  - › Number, standards and types of devices is **growing** rapidly.





# INTRODUCTION

## RF DESIGN CHALLENGES

- Iterations



- › Generally the longest time, not to mention cost, for a single iteration is the prototype fabrication time.
- › Reduced number of design iterations is necessary to meet time-to-market expectations.
- › Improved simulation accuracy is required in order to reduce the number of iterations, yet the number of design passes to meet the specification has not changed substantially over the last 20 years.

- Tools

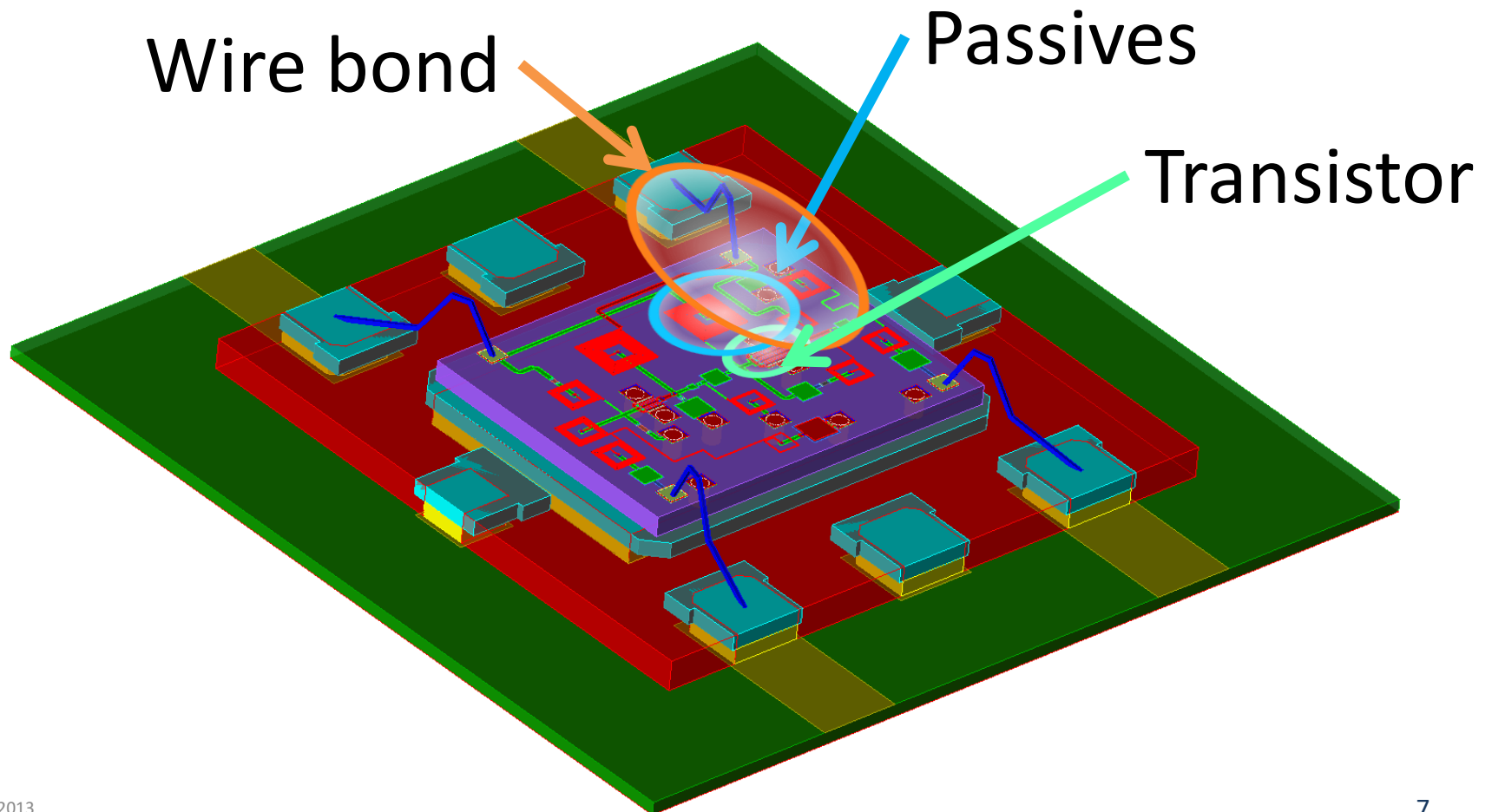


- › Electronic Design Automation (EDA) has roots in two basic approaches:
  - Circuit Simulators
  - EM Field solvers
- › To overcome the limitations of both, EDA tools have incorporated the ability to paste in blocks of simulation results to permit “co-simulation” of circuit and EM results.
- › This approach is limited in its ability to accurately simulate circuit response and hence has not reduced the number of design cycles.



# INTRODUCTION

## RF DESIGN CHALLENGES





✓ Introduction

➤ **EM-Supreme<sup>®</sup> Overview**

Design Flow

PA Example

RF Power Transistor Application

Summary

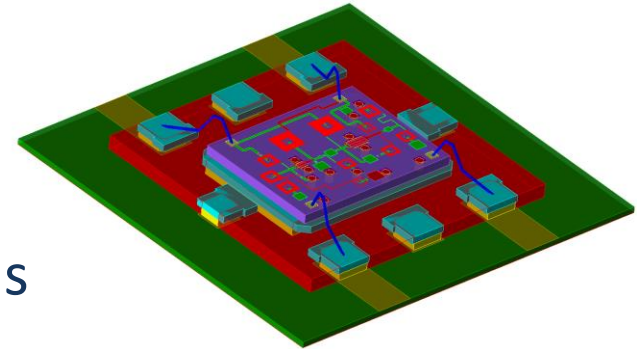




# EM-SUPREME<sup>®</sup> OVERVIEW

## EM-SUPREME<sup>®</sup>

- Finite Difference Time Domain (FDTD) model that uses no approximations.
- The tool models electromagnetic fields as they pass through the active and passive components to predict real circuit performance as it physically happens.
- Allows incorporation of the IC, passives, substrate and package in the model.
- Compatible with existing design tools to minimize learning curve.
- Two modes of operation:
  - › **Stand Alone** – Provides all necessary tools to completely model a given component or module.
  - › **Optimization** – Adds functionality to existing tools to improve prediction of the actual circuit performance.





# What Exactly Can go Wrong

## Transistor Models?

- Circuit-Based
- Measurements-Based with/without Quantum Mechanics correction-terms (through *curve fitting* or *NN*) .
- Models that take the EM distributed effects into account (possibly mm-wave frequencies) and PDK's
- You need to have a smart engine to choose between any of these models.
- Models have to be general.



# EM Sample Problems

- *Coupling of EM and transistor* (through radiation for example) if you have distributed effects. The transistor is nonlinear so this effect is more pronounced specially for transient response and high-power high-frequency devices (GaN, LDMOS, etc).
- Possibility of coupling is everywhere (e.g. wire-bond, laminate multilayer, on chip spirals, you name it).

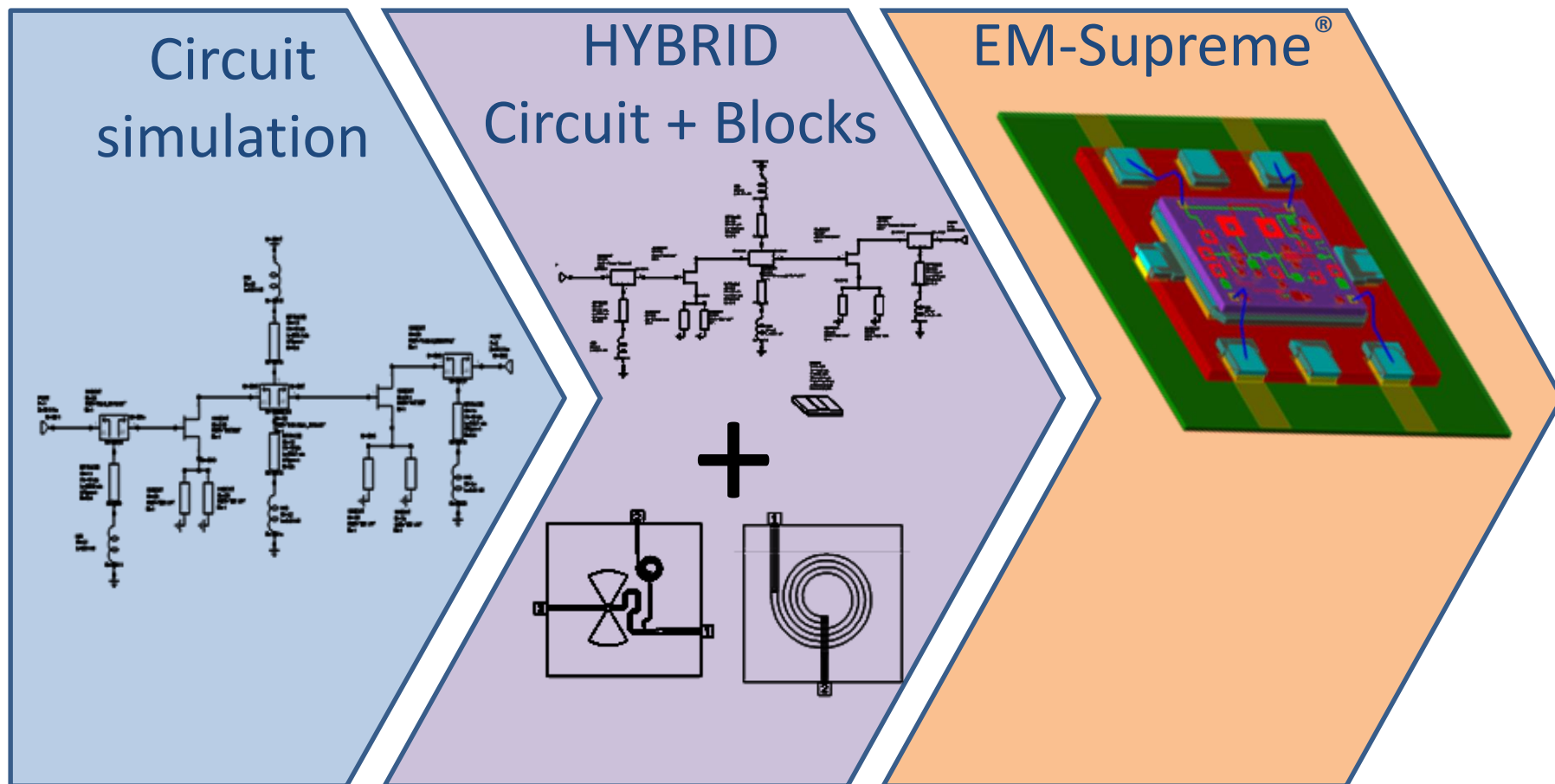


# EM Sample Problems

- Mold simulation and coupling of EM-reflecting back from *laminare mold* into the IC. It's very important to look at the *transient response* of this. The only way to see the effect of model is to have a full simulation of the entire chip.
- *Magnetic coupling loops* (for example before and after a PA). The length of loops is changed as you add a transistor and may result to an unintended magnetic coupling.
- Coupling with noise in switching power supplies.



## EVOLUTION / ACCURACY





## EM SIMULATOR COMPARISON



Company	PedaSoft	Sonnet	CST	Ansys	Zeland	IMST
Product	EM-Core <sup>®</sup>	Sonnet	CST-Ems	HFSS	IE3D	Xccel
Geometry	2.5 & 3D	2.5D	3D	3D	3D	3D
Method	FDTD	MoM	FIM	FEM	MoM	FDTD
Time Domain	√	X	√	X	X	√
Freq Domain	X	√	√	√	√	X
Accuracy	High	Medium	High	High	High	High
Memory	Medium	Medium	High	High	Medium	High
Speed	Medium	Fast	Medium	Medium	Medium	Fast
Shielded	√	√	√	√	√	√
Radiated	√	X	X	√	X	X
DXF	√	√	√	√	√	√
Customizable	√	X	X	X	X	X
Cost	Low	Medium	High	High	Medium	Medium



## SYSTEM SIMULATOR COMPARISON

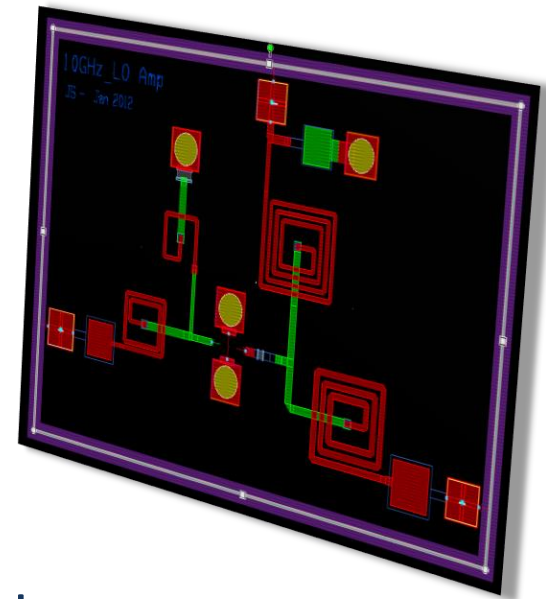


Company	PedaSoft	KeySight	AWR	Ansys
Product	EM-Supreme®	ADS + Momentum	MWO + AXIEM	Nexxim + HFSS
Geometry	2.5 & 3D	2D	2.5D	3D
Method	FDTD	FEM	MoM	FEM
Time Domain	√	X	X	X
Freq Domain	X	√	√	√
Circuit EM Hybrid	√	√	√	√
Active EM Hybrid	√	X	X	X
Circuit + Active EM	√	Co-simulation	Co-simulation	Co-simulation
Active Models	Unlimited	Limited	Limited	Limited
Accuracy	High	Medium	Medium	High
Memory	Medium	Low	Medium	High
Speed	Medium	Fast	Fast	Medium
Shielded	√	√	√	√
Radiated	√	X	X	HFSS Only
DXF	√	√	√	√
Customizable	√	X	X	X
Cost	Medium	High	High	High



## EM-SUPREME<sup>®</sup> ADDITIONAL FEATURES

- Layout can be dissected to look at:
  - › Coupling
  - › Isolation
  - › Interference
- Transient Analysis of Sub-circuits
- Tx / Rx Path Multi-tone Analysis
- Load Pull / Source Pull
- Gain & Harmonics
- Radiation
- Software can be customized to meet specific customer requirements.





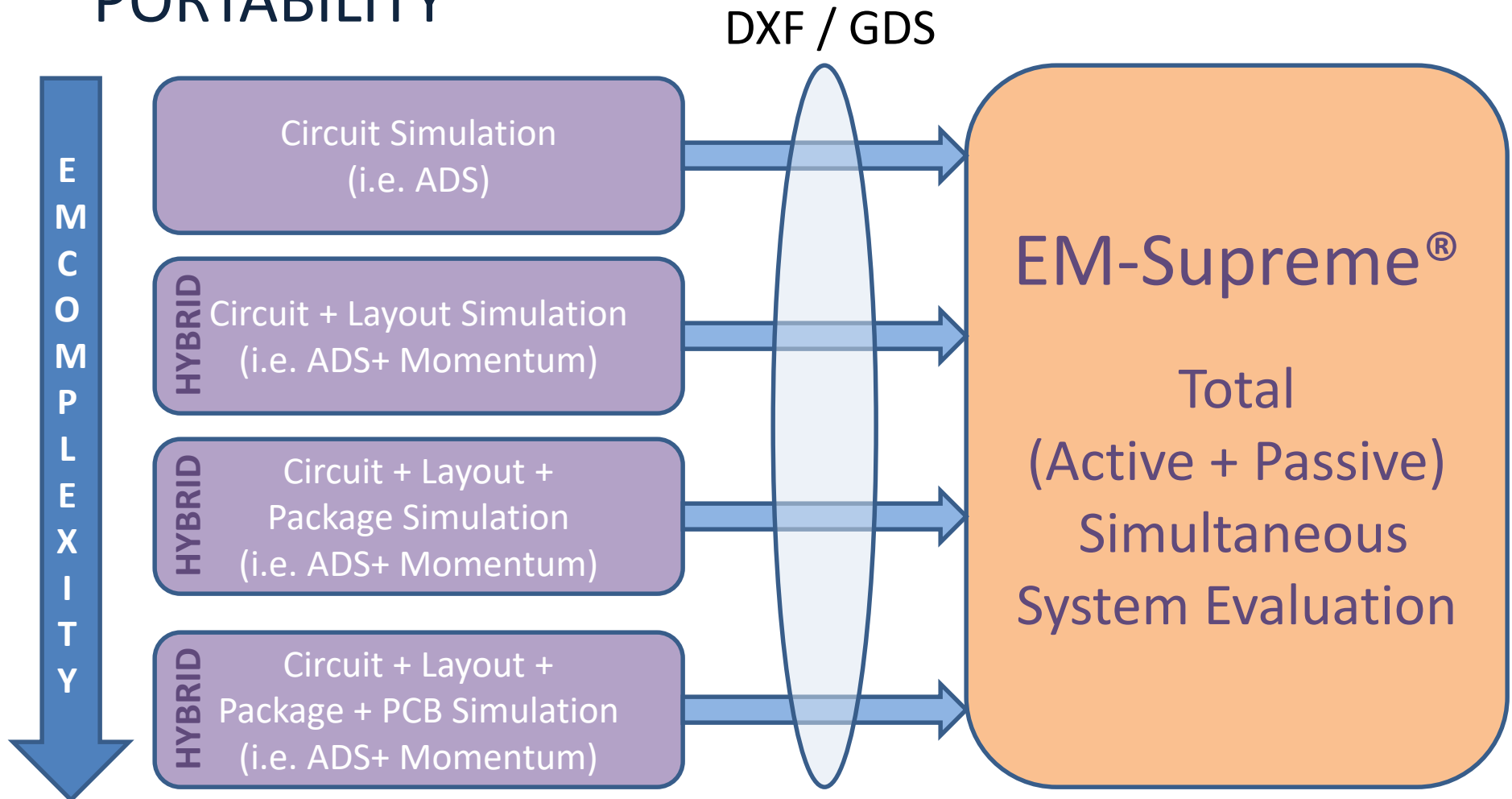


- ✓ Introduction
- ✓ EM-Supreme<sup>®</sup> Overview
- **Design Flow**
  - PA Example
  - RF Power Transistor Application
  - Summary



# DESIGN FLOW

## PORTABILITY

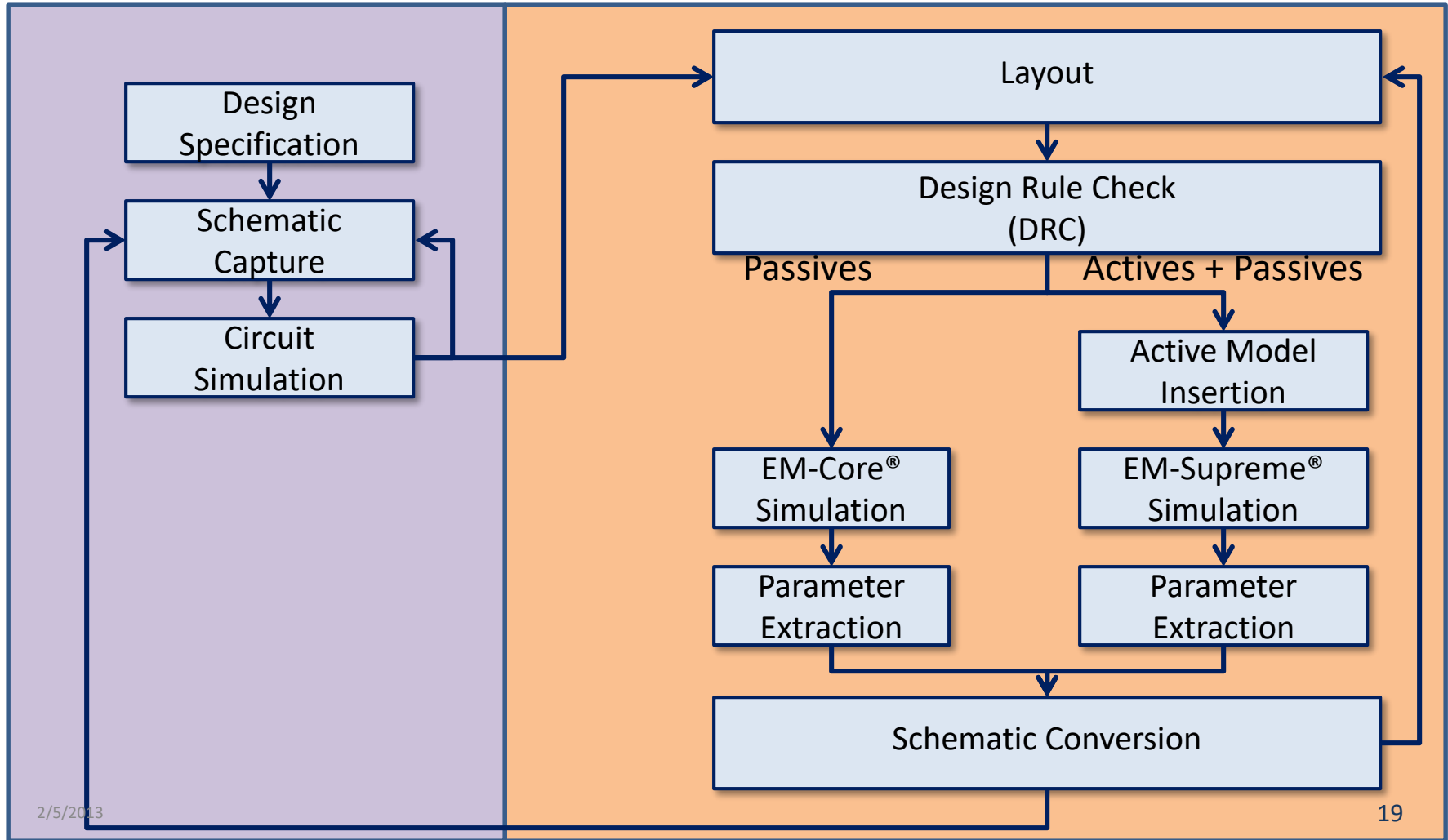




# DESIGN FLOW

## STAND ALONE MODE

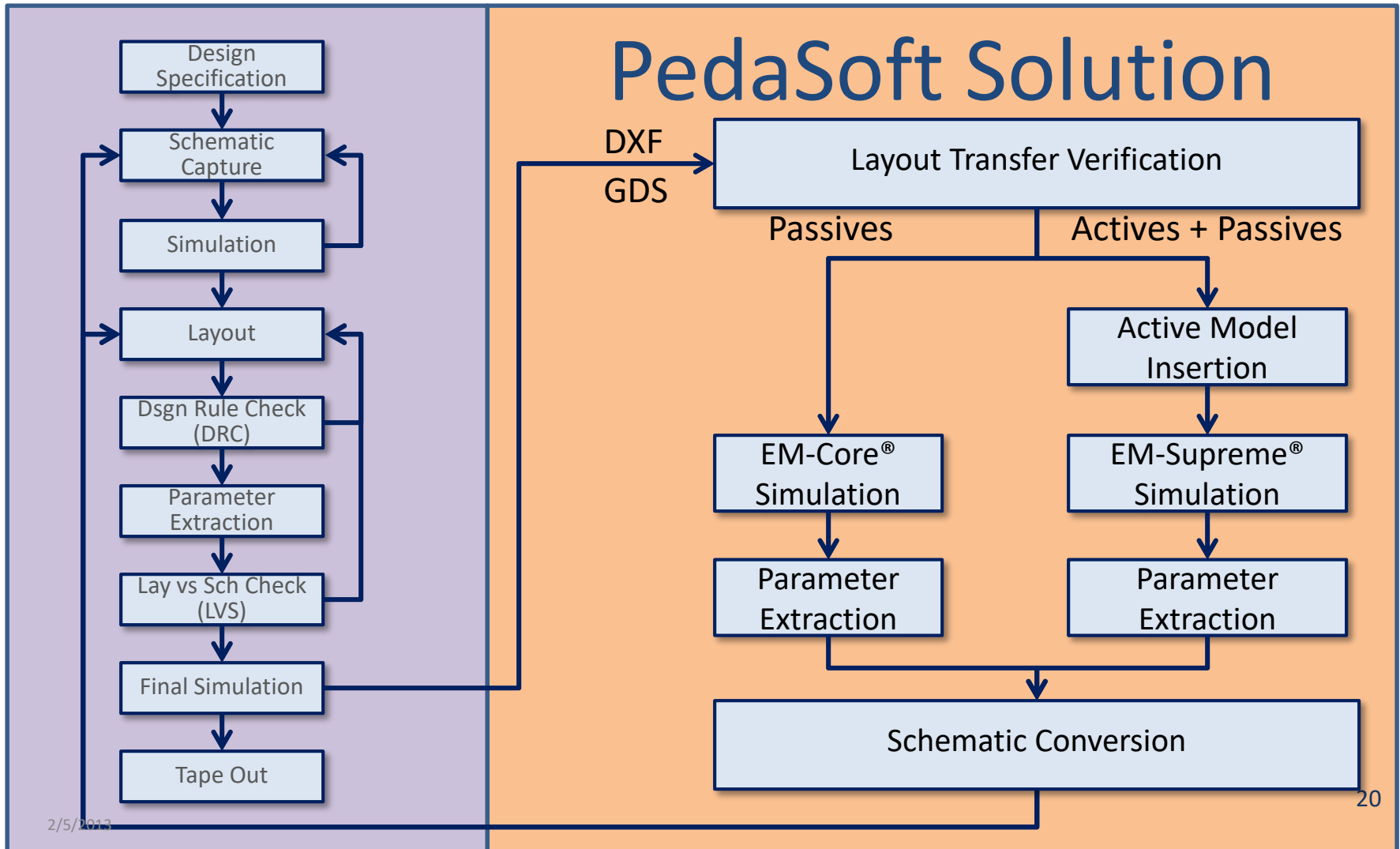
## PedaSoft Solution





# DESIGN FLOW

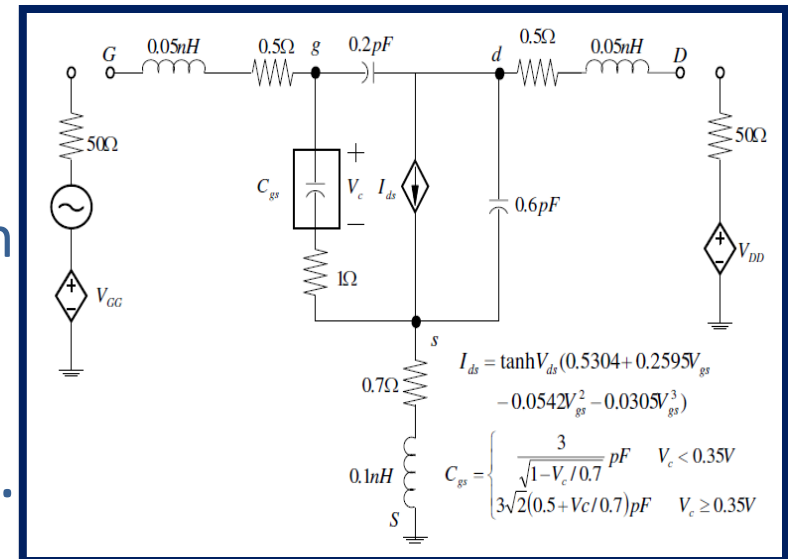
## OPTIMIZATION MODE





## ACTIVE MODELS

- EM-Supreme® can accept any model:
  - › Spice, Curtice, Angelov, Stats-Pucel, ...
  - › Foundry PDK, TOM, Customer proprietary, ...
  - › Measurement-based / Temperature dependent / ...
- PedaSoft customized
  - › PedaSoft will take any of the above models and work with the manufacturer / foundry to optimize the model for best results in EM-Supreme®.





- ✓ Introduction
- ✓ EM-Supreme<sup>®</sup> Overview
- ✓ Design Flow

## ➤ **PA Example**

RF Power Transistor Application

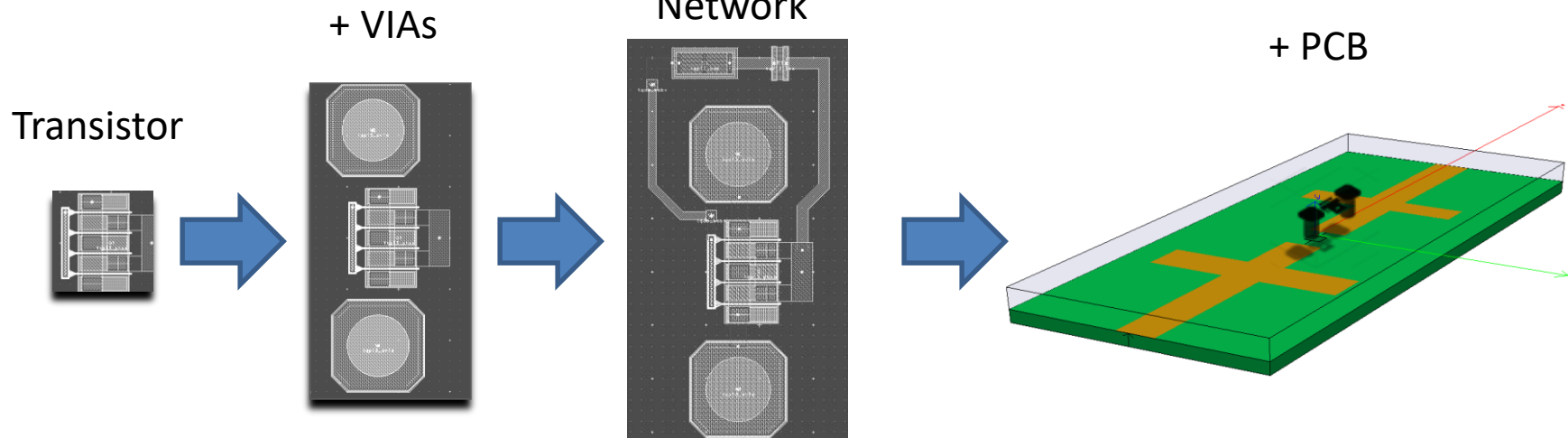
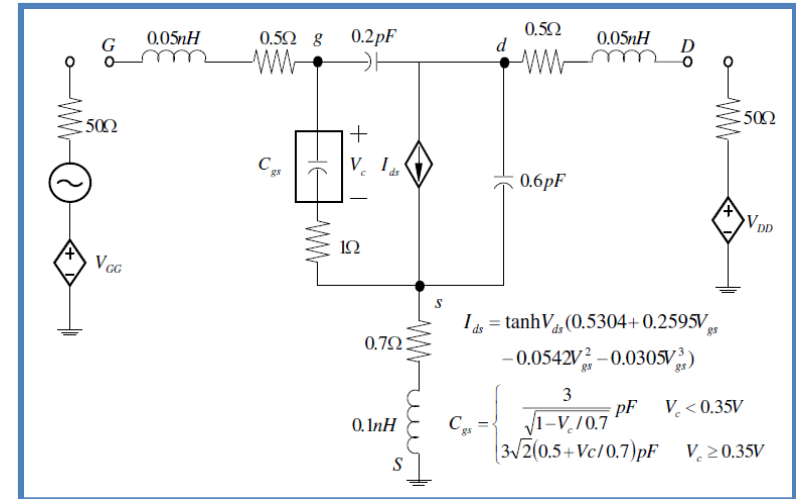
Summary



# EXAMPLES

## PA DESIGN

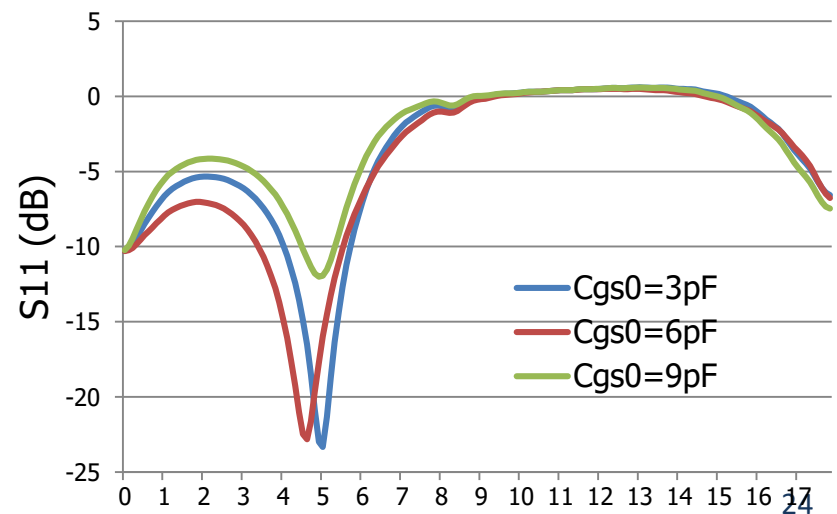
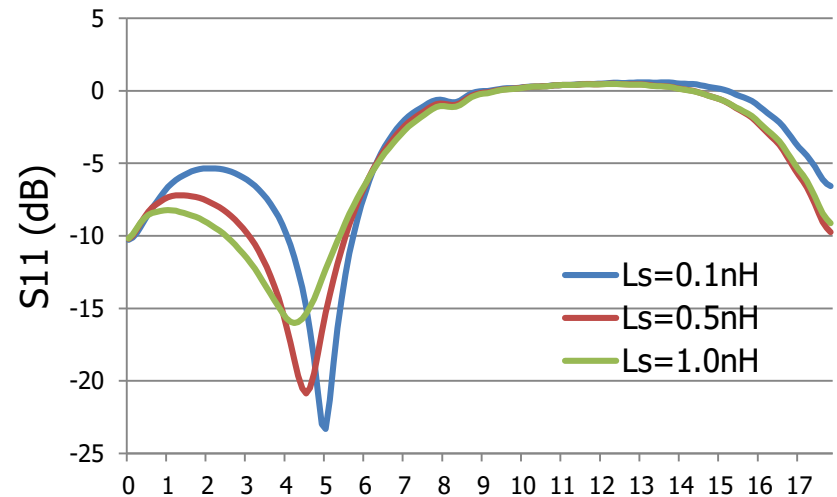
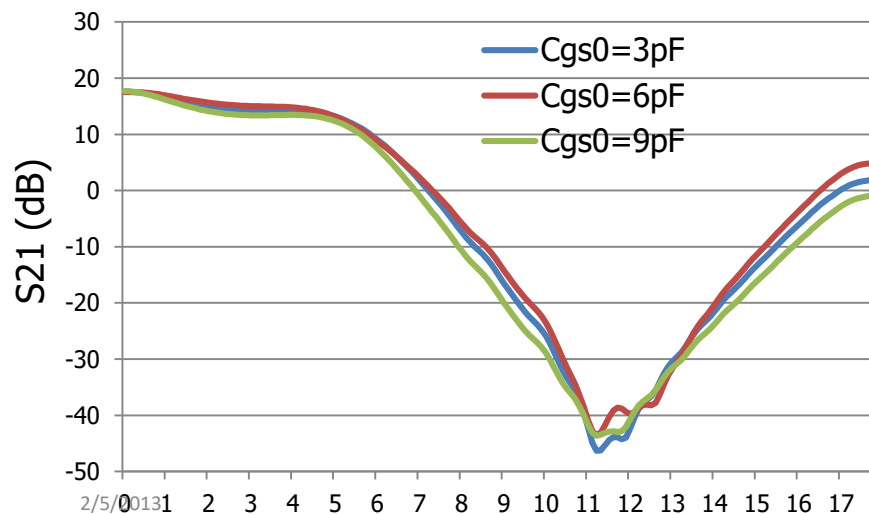
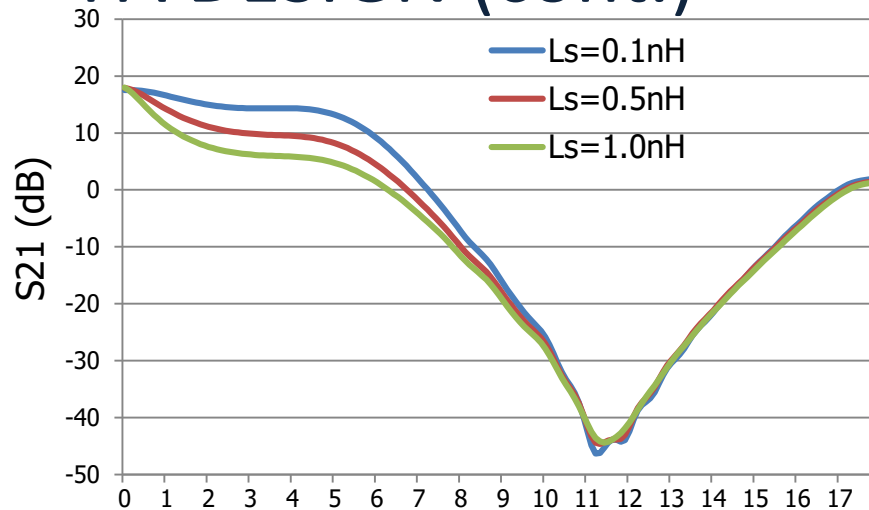
2 – 5 GHz flat gain target





# EXAMPLES

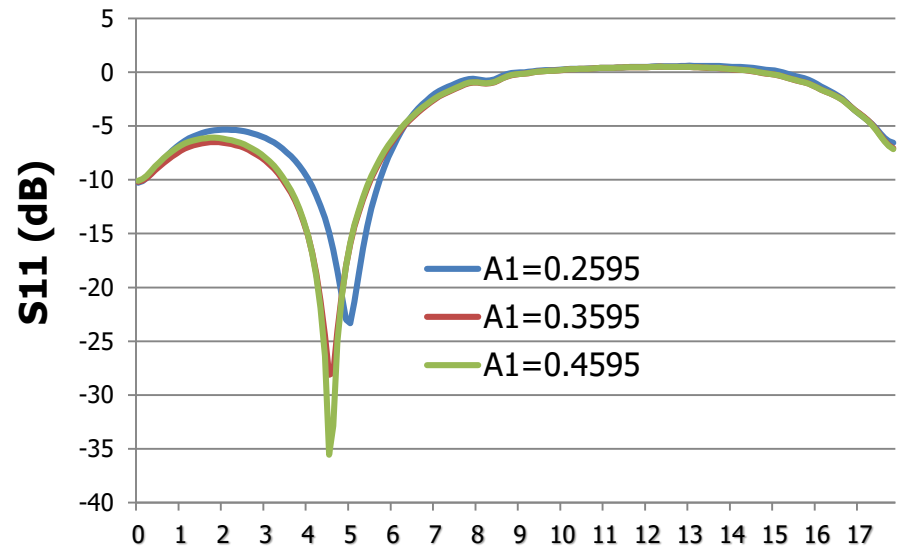
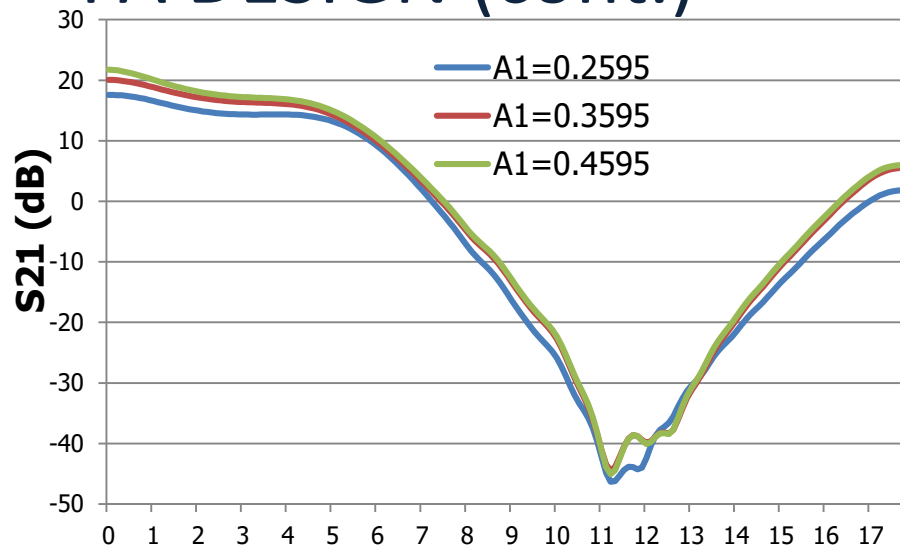
## PA DESIGN (cont.)



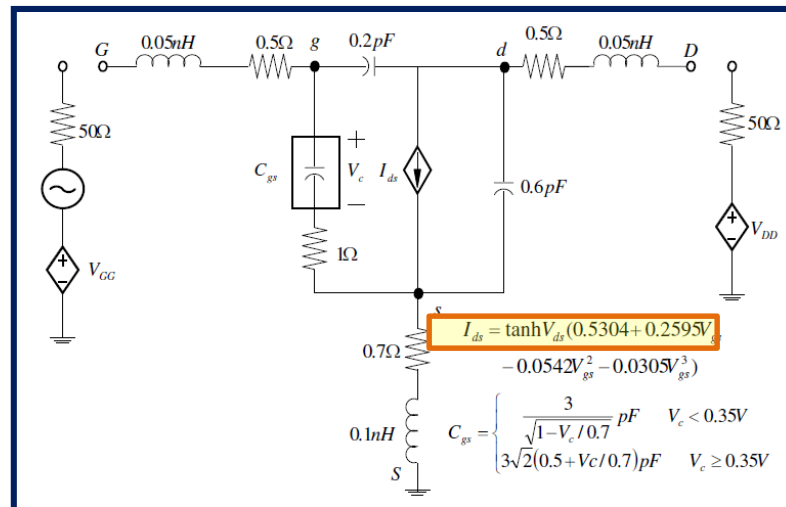


# EXAMPLES

## PA DESIGN (cont.)



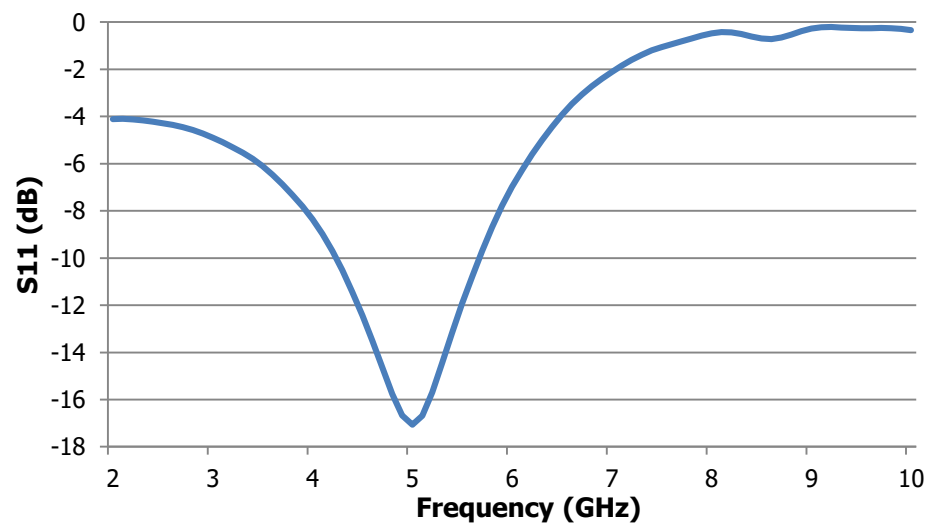
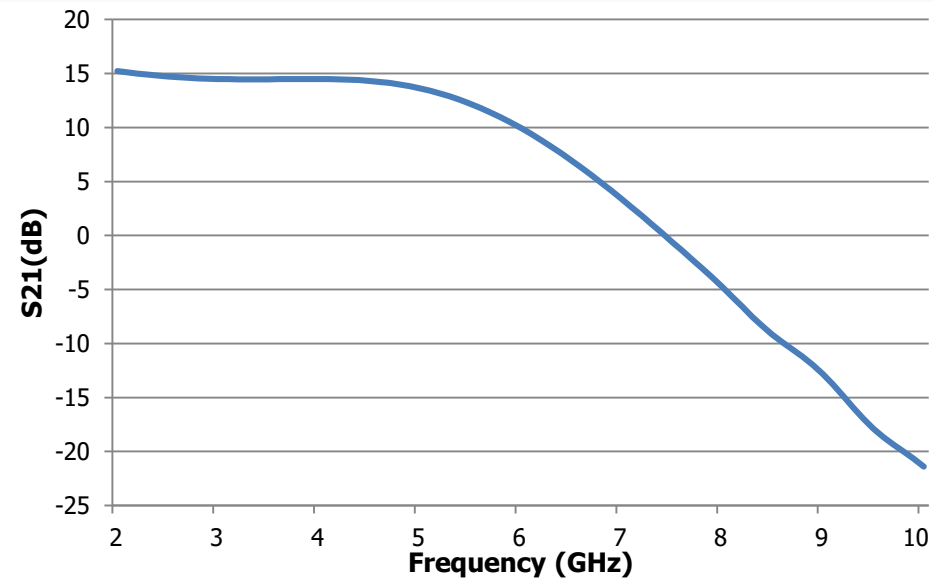
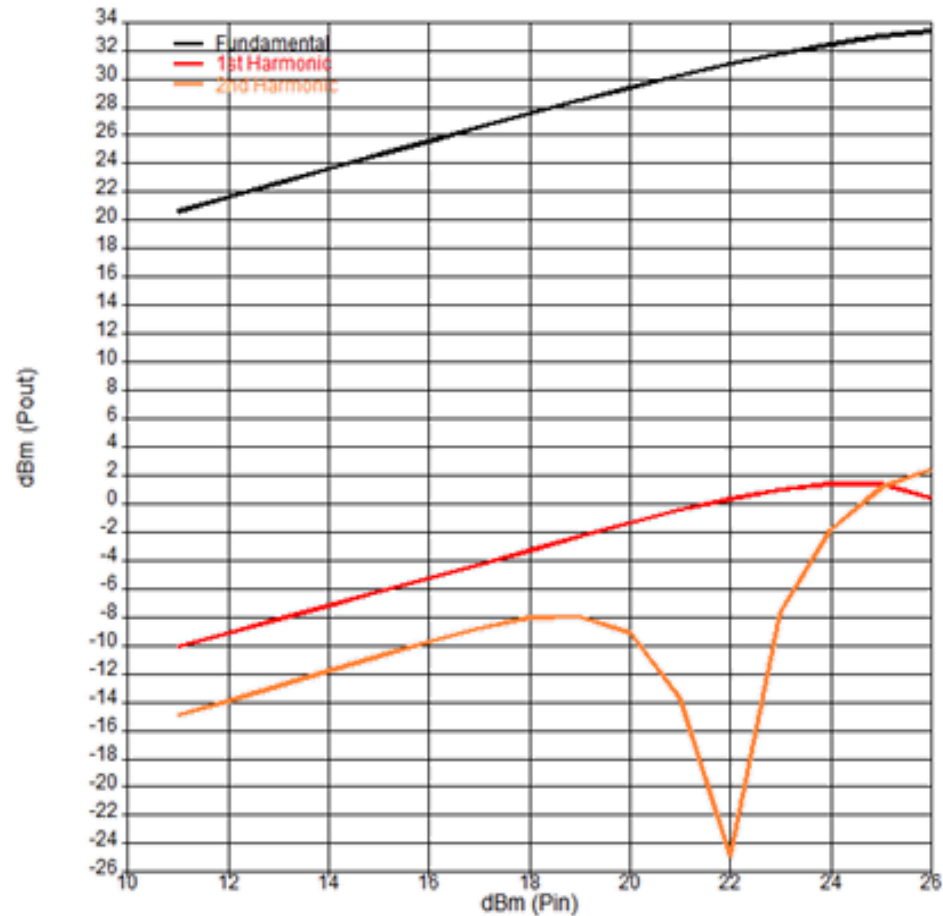
Endz	510.000
From Metal	Square5
To Metal	Square6
Source Impedance	50.000
Load Impedance	50.000
Cgs0	3.000
Cgd	0.200
cds	0.600
Ls	0.100
Lg	0.050
Ld	0.050
A0	0.5304
A1	0.2595
A2	-0.0542



A3	-0.0305
Alpha	1.000
Ri	1.000
Rs	0.700
Rg	0.500
Rd	0.500
VGG	-0.810
VDD	18.960
Signal Simulations	Large
Temperature	300.000
Power Sweep (dbm)	10.000
Power Sweep Min (dbm)	0.000
Power Sweep Max (dbm)	30.000
Input Frequency (GHz)	6.000



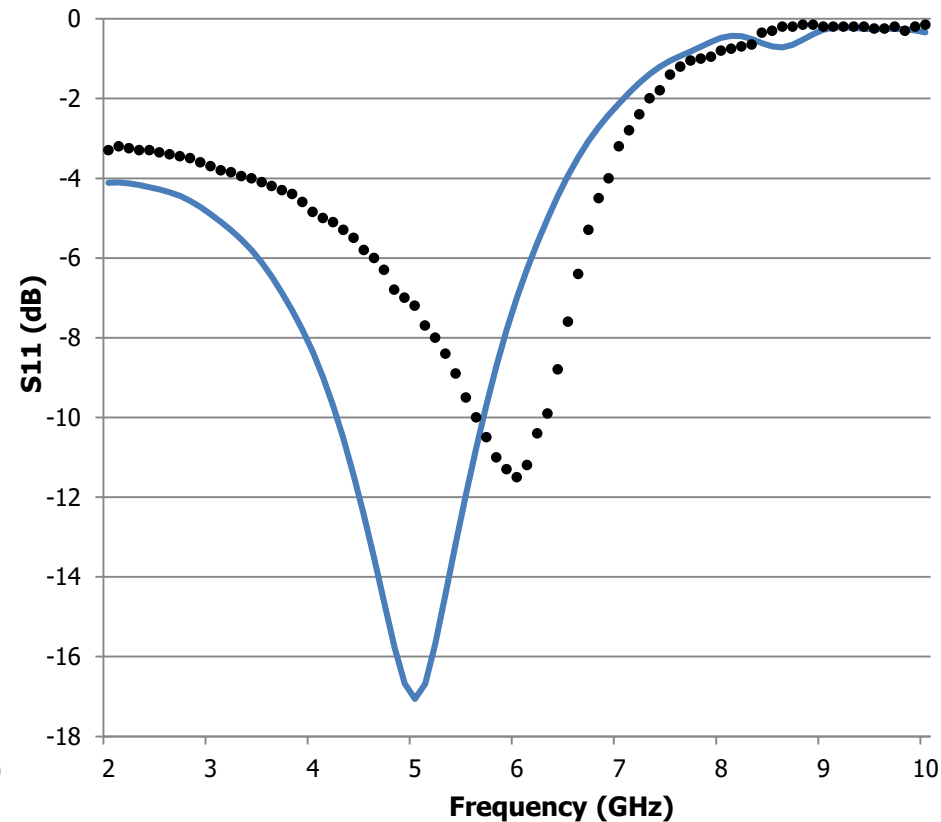
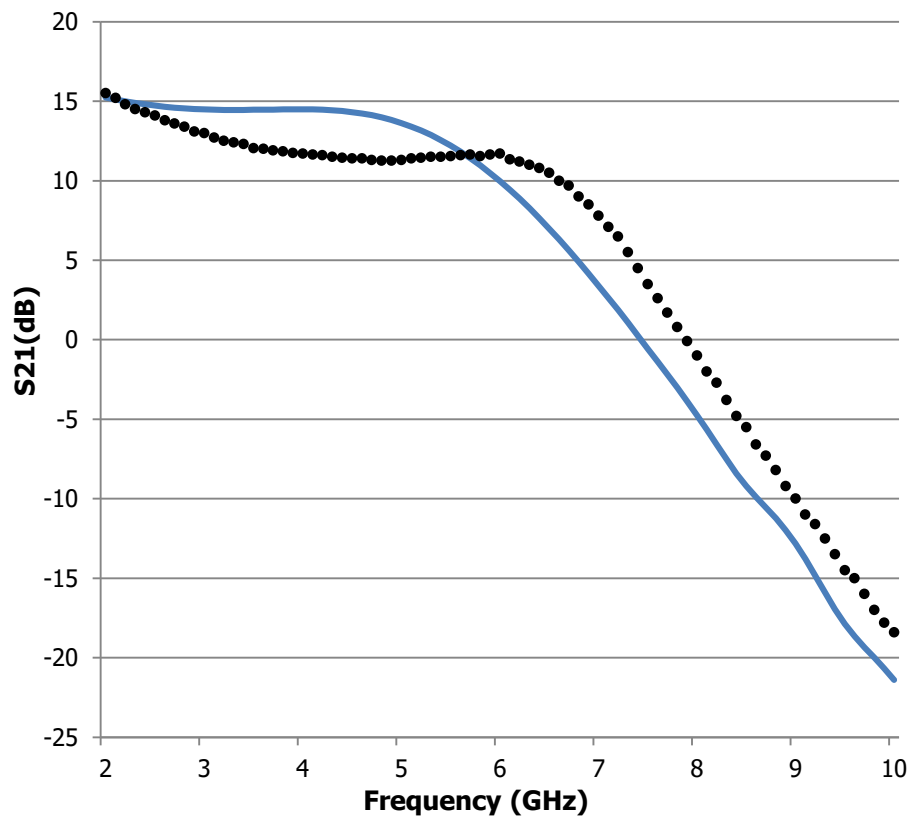
## PA DESIGN (cont.)





## PA DESIGN (cont.)

- Comparison of same circuit using co-simulation





- ✓ Introduction
- ✓ EM-Supreme<sup>®</sup> Overview
- ✓ Design Flow
- ✓ PA Example
- **RF Power Transistor Application**
- Summary



**PEDASOFT**

# NUMBER OF W/B's & LENGTH

PedaSoft EM Supreme Trial v9.00 - BondwIRE

File Edit Add Item View Chip Designer Options Windows Help

Model Simulation Results Radiation Pattern

Max (mm) = 0.50564986

Dx (mm) 0.40640000

Dy (mm) 0.26499999

Dz (mm) 0.42330000

Domain Properties

Name	Box1
lx	24.384
ly	4.240
lz	25.398
lh	0.795
epr	2.200
Xgrid	60.000
Ygrid	16.000
Zgrid	60.000

Component Properties

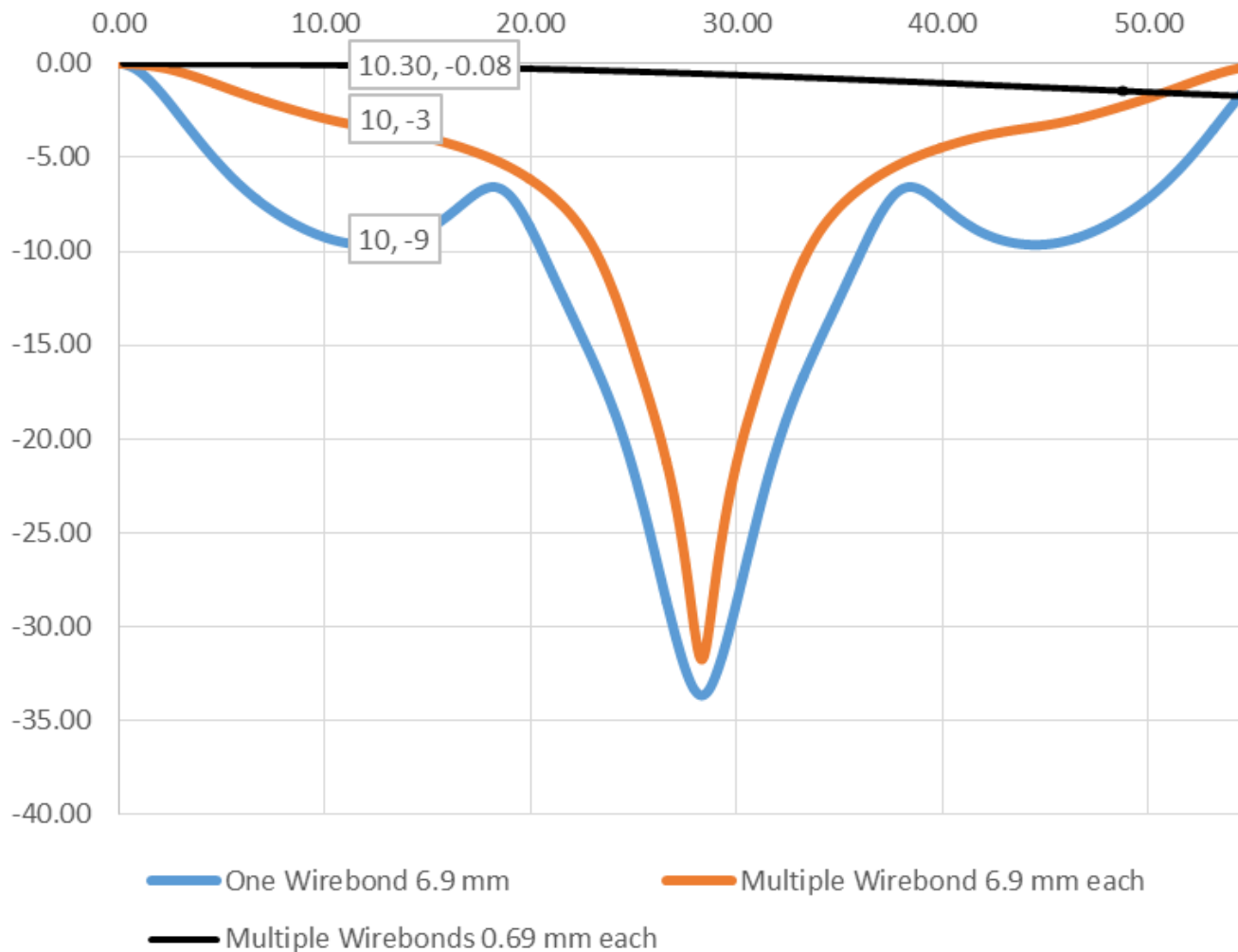
Name	
Startx	
Starty	
Startz	
Endx	
Endy	
Endz	
From Metal	Square1
To Metal	Square2

Hold left mouse down and pan shape in any direction



# S21 XMISSION LINE ANALYSIS

**S21 (dB) Versus Frequency (GHz)**

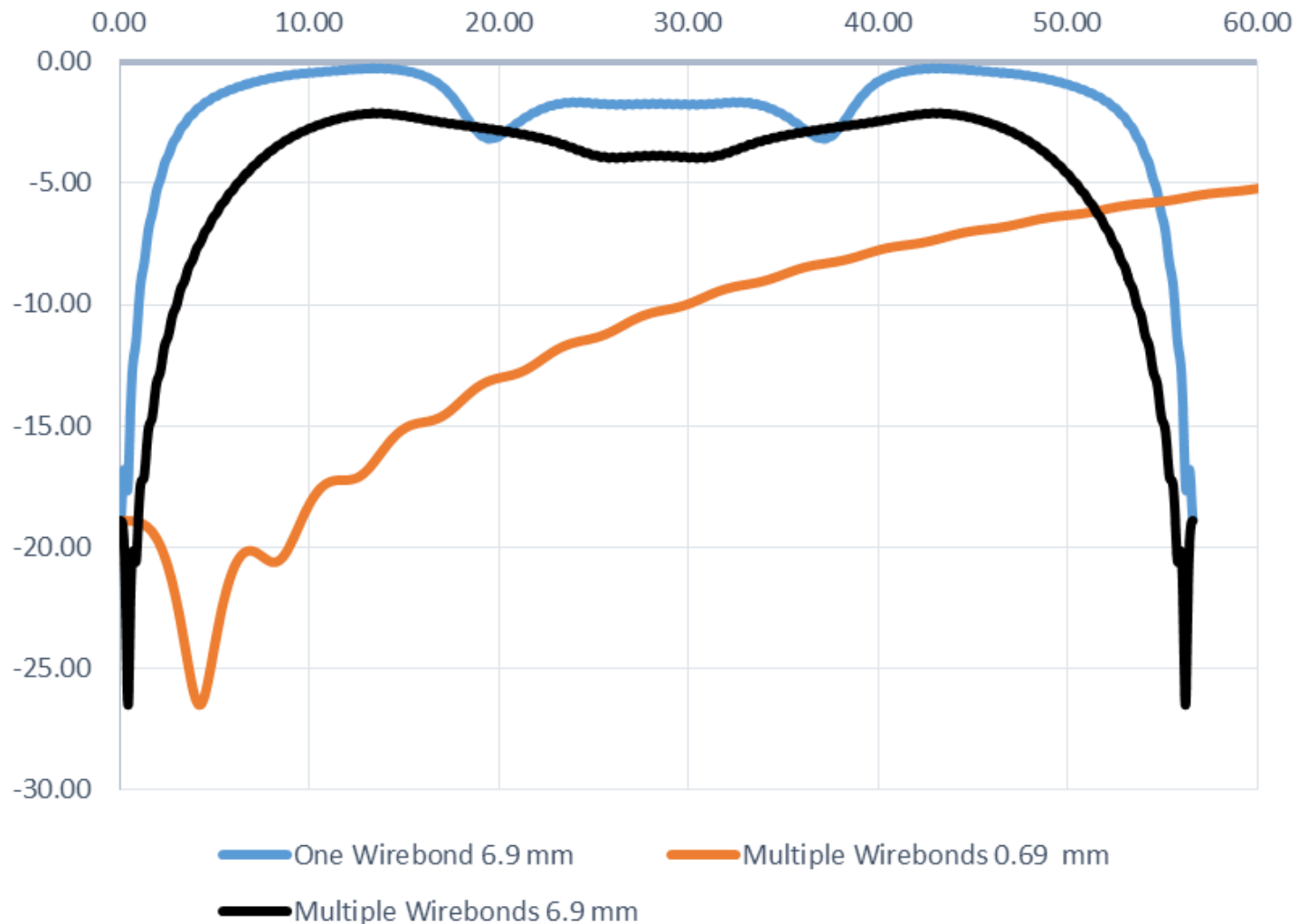




**PEDASOFT**

# S11 XMISSION LINE ANALYSIS

$S_{11}$  (dB) versus Frequency (GHz)





# W/B CONCLUSIONS

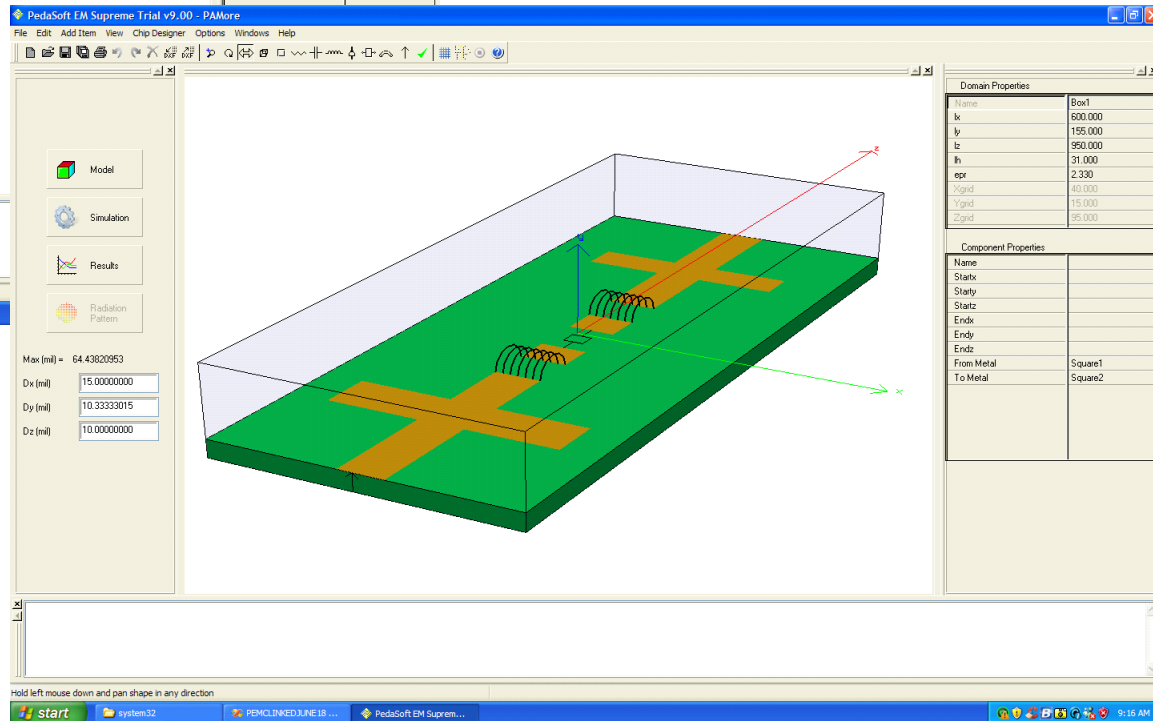
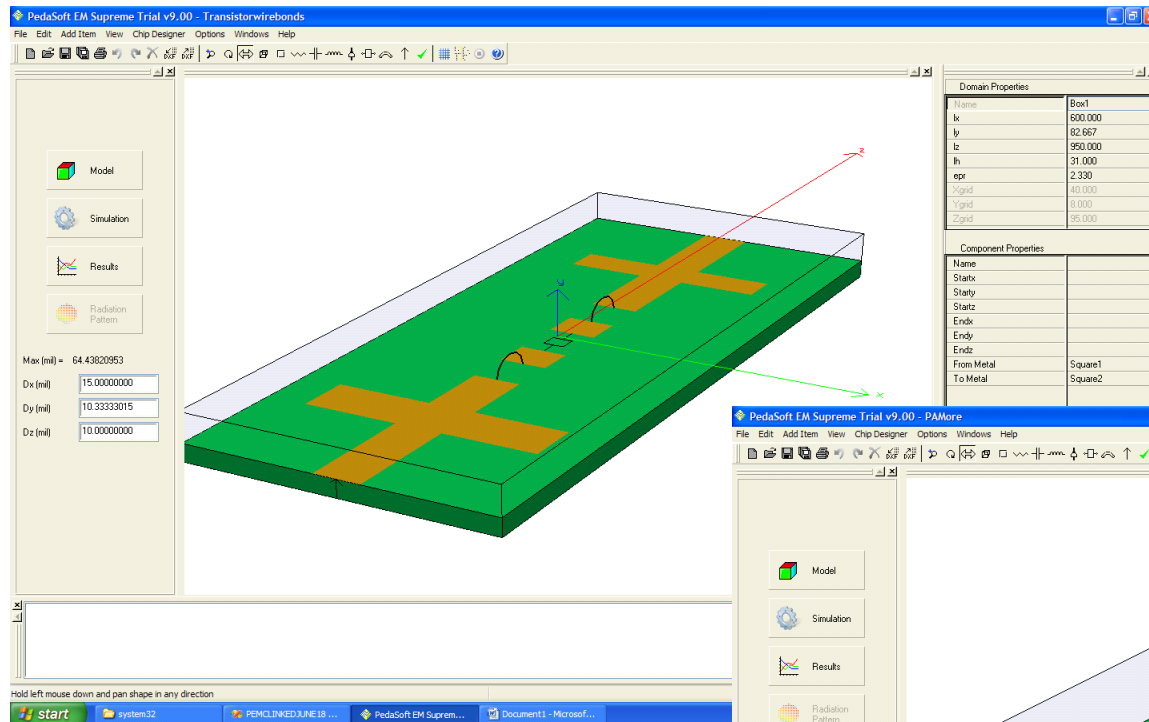
- Smaller wire lengths are better since they provide lower inductances and therefore their effect is dominating only at higher frequencies.
- Multiple wires are better since they provide lower inductances and impedances and therefore will have better Insertion Loss for L-Band (1-2 GHz), S-Band (2-4 GHz) , and up to C-Band (4-8 GHz).
- The structure is resonating somewhere in the 30 GHz band for 6.9 mm wires so it should not be used for either K and Ka Band (18-40 GHz)
- Multiples wires should be used in the mid X-band (~10 GHz) over single wires
- 0.69 mm wires should be used for V-Band (75-110 GHz)





**PEDASOFT**

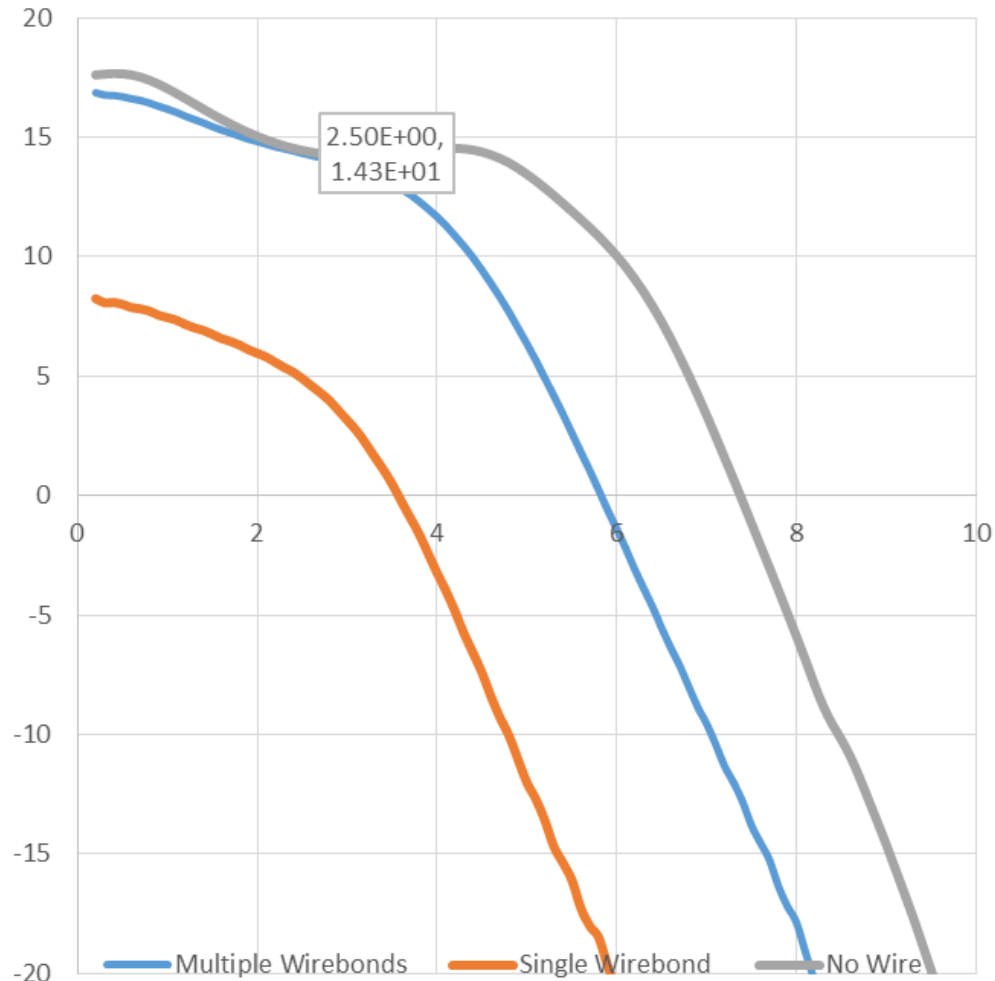
# NUMBER OF W/B's ANALYSIS





# S21 ANALYSIS

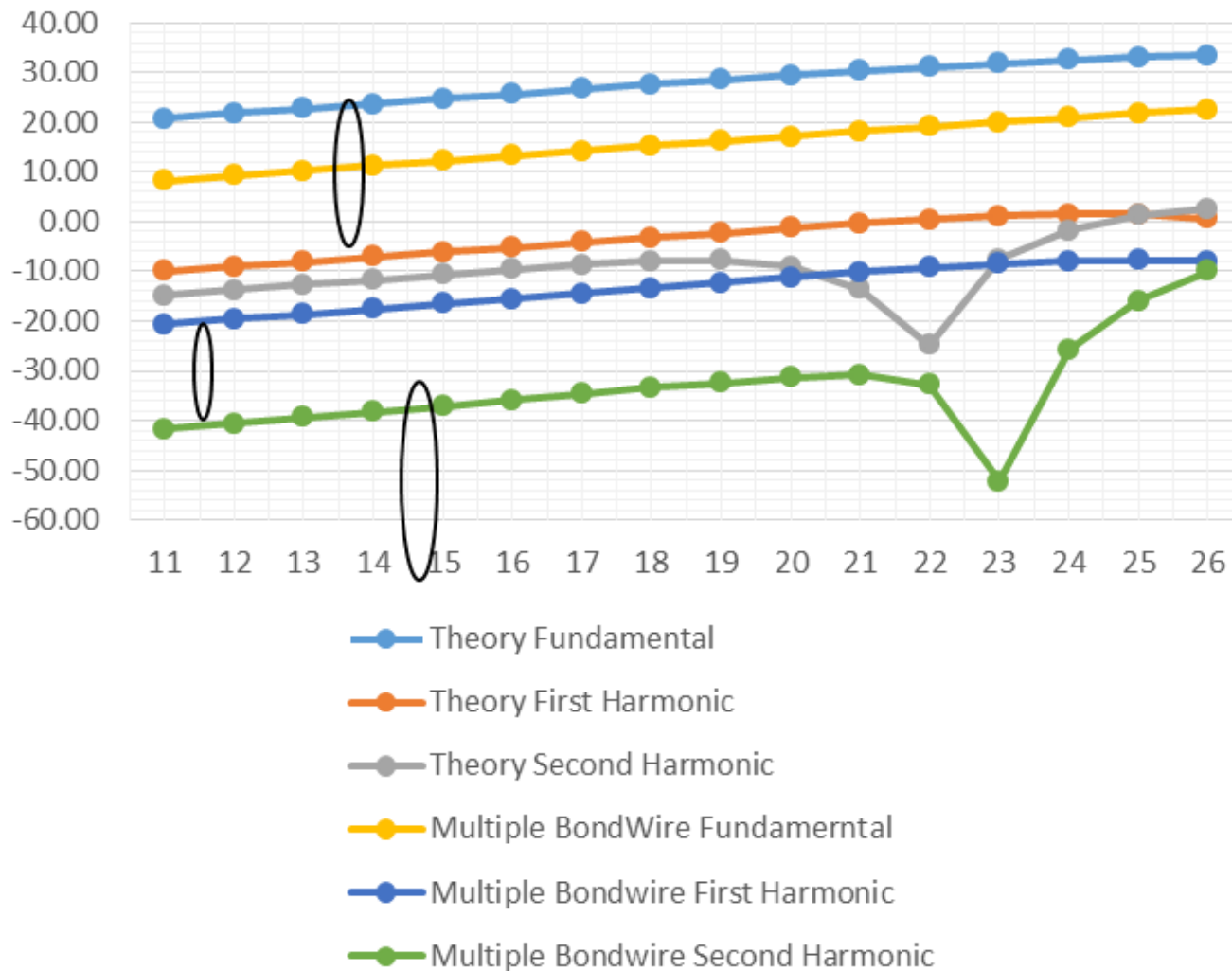
Gain (dB) Versus Frequency (GHz)





# W/B $f_n$ EFFECTS

Input Power Versus Output Power (dBm)





# W/B CONCLUSIONS

- Adding a single wire on both sides of the transistor drops the gain by 10 dB.
- Adding multiple wires of the same length optimizes the gain for L- and S-bands “i.e. up to 4 GHz.”
- For frequency  $> 4$  GHz, the gain reduces dramatically which emphasizes the need to optimize the structure by reducing wire lengths and possibly employing different wire shapes.
- Gain as well harmonics can all be optimized by PedaSoft’s EM-supreme using several variations including wire shape, number, and length as well as transistor technology and passive manifolds around the PA.



PEDASOFT

# RF POWER TRANSISTOR

PedaSoft EM Supreme Trial v9.00 - PAMore

File Edit Add Item View Chip Designer Options Windows Help

Model  
Simulation  
Results  
Radiation Pattern

Max (mil) = 64.43820953  
Dx (mil) 15.00000000  
Dy (mil) 10.33333015  
Dz (mil) 10.00000000

High  $P_{out}$

Large Dimensions

Signal Interaction

PDK, simulation or actual structure

Domain Properties

Name	Box1
lx	600.000
ly	155.000
lz	950.000
lh	31.000
epr	2.330
Xgrid	40.000
Ygrid	15.000
Zgrid	95.000

Component Properties

Name	
Startx	
Starty	
Startz	
Endx	
Endy	
Endz	
From Metal	Square1
To Metal	Square2

Hold left mouse down and pan shape in any direction

start system32 PEMCLINKED JUNE18 ... PedaSoft EM Suprem...

9:15 AM



## POTENTIAL PROJECTS

Hardware Company1 – wants a MOSCAP model for customers

Hardware Company 2 – wants an effective simulation solution

PedaSoft – wants to extend its model and develop a more comprehensive capability to accurately address this market.



- ✓ Introduction
- ✓ EM-Supreme<sup>®</sup> Overview
- ✓ Design Flow
- ✓ PA Example
- ✓ RF Power Transistor Application
- Summary



# SUMMARY

There are endless possibilities of EM coupling and radiation that need to be modelled for transistors embedded. Therefore a complete and full EM solution should be employed. Examples of EM coupling include but not limited to:

- Coupling between bond-wires on the PA input-side as well as between wires at input and output sides of the same PA and different PA's
- Coupling between the Gate and Drain as well as Gate/Drain bond wires blocks
- Coupling between Gate, Drain, Source as well as bond-wires

EM-Supreme imports the models of MOSCAP as well as the PA and then the passive manifolds are created or imported as DXF. The whole structure is simulated including the PA and passives in one run using full wave model. The PA and MOSCAP models can be based on any of the following:

- Measurements (behavior)
- Foundry
- Model can be functions of dimensions A,B,C, etc as well as temperature and power dependent
- New models developed





For EM-Supreme Download or Support or to enquire about steps required to engage with our *RF design services*, feel free to call or email us at:

[support@pedasoft.com](mailto:support@pedasoft.com)

+1(650)352-3585

THANK YOU!